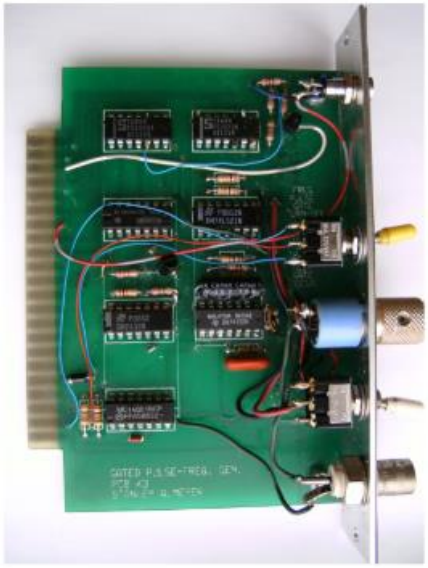
Stanley Meyer's **Gated Pulse Frequency Generator** Functional Description

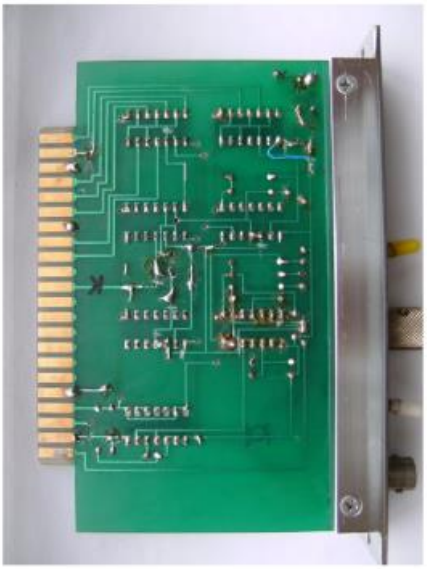
This document is a functional analysis of the Gated Pulse Frequency Generator. The purpose was to better understand its role in the Stanley Meyer's water cell system and what function does it perform.

Simple answers:

1. Switch on front panel turns on/off frequency signal going to cell by stopping output of IC SN7408N
2. Switch on front panel select either:
    a. Manual mode - signal comes from Main Frequency Generator card or
    b. Accel - signal comes from Accelerator Module or another external source
3. Signal Potentiometer sets width of frequency pulses in following range 3.102msec to 36.102msec. Note: this setting applies to both frequency sources.
4. Provide an interface to let other modules turn off the cell Input (K)
5. Outputs adjusted signal to VIC Module
6. Does not appear to add the off Gate seen in the VIC signal

Main purpose appears to be to set a minimum pulse with on frequency signals (the gate) and provide a means to adjust it.





Picture and circuit are from Stanley Meyer's estate above and circuit diagram below. Note the first 2 IC are 7402 (s)

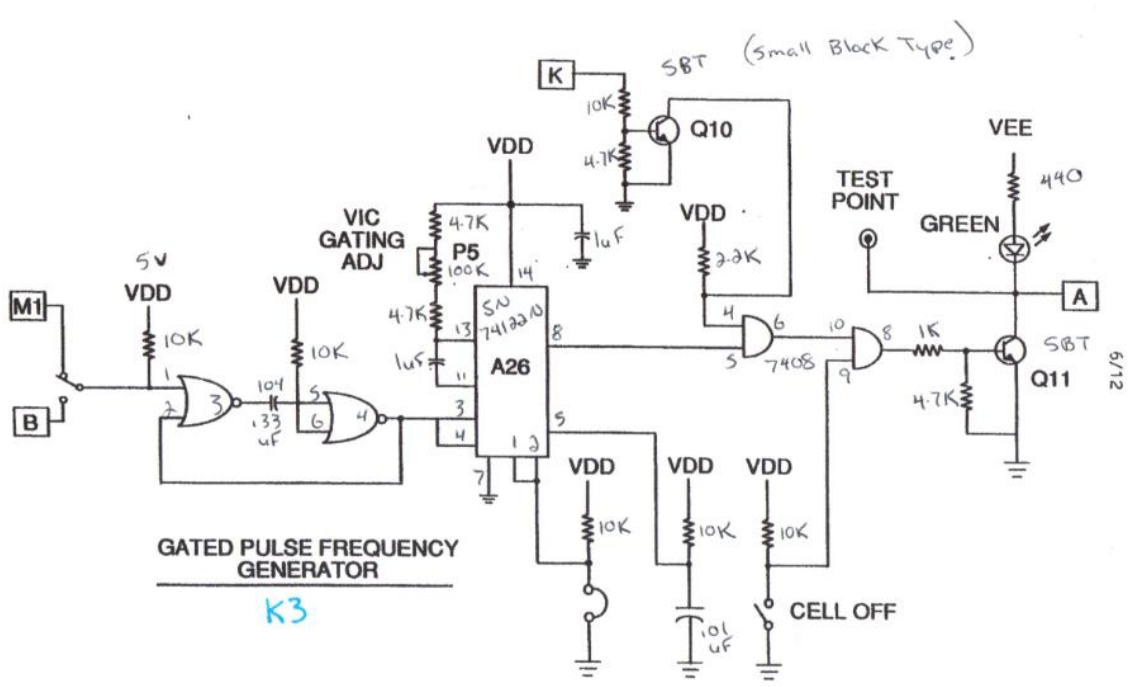


FIGURE 6

Inputs to card:

1. 5 VDC to drive the electronic (VDD) on circuit diagram
2. 10 VDC (VEE) to provide power to Green LED on front panel
3. Switch on front panel to turn Cell On/OFF
4. Pot 100 K ohms on front panel to adjust pulse width labeled **L H.** It's the 100 K ohms pot (Labeled VIC GATING ADJ on circuit)
5. Switch on front panel to select Man Input (B) or Accel Input (M1) from other cards
6. Input (K) from Gas Feedback Control Module (Allows external module to shut off cell)
7. Fuse on ground to protect IC A26 (SN 74122N)

Outputs from card:

1. Gated signal (A) to VIC module (Gated here means pulse width has been set)
2. Gated signal to light the Green LED on panel
3. Test point on panel

Functional Description of Circuit

The resisters and IC on the card are used to bias the ICs and will not be discussed with the exception of the 100K Pot. Other items will be covered left to right as input signal enters on left and leave on right with exception of input K which comes in as a bias from the top.

Input (B) is from the Main Frequency Generator Board and is one of the 4 frequencies that are generated on that card.

Input (M1) is from the Digital Control Means Module. For this analysis it is assumed input will be in the same range as can be provided from the Main Frequency Generator Board.

The first two ICs on left are in a 7402 chip which contain 4 NOR ICs only 2 are used. They are used in this circuit as and S-R Latch (Flip-Flop). See https://www.youtube.com/watch?v=mo4Lq0DvJ68 for good explanation of what they do as most data sheets do not explain why they are used. Simple explanation is they perform 2 functions 1) clean up the leading and training edges of the pulse to remove any noise in signal and 2) maintain the signal input at correct level for the SN74122N. NOTE as explained in the video NOR ICs can latch both the 0 and 1 states of the signal.

IC SN74122N sets the size of pulse which is determined by the 100K Pot. This allows the size of the pulse width to be controlled from front panel 100K pot.

> From data sheet:
> **Retriggerable Monostable Multivibrator Pin Function:**
> An external timing capacitor may be connected between Cext and Rext/Cext. For accurate repeatable pulse widths connect an external resistor between Rext/Cext and Vcc leaving Rint open [unconnected]. To obtain variable pulse widths connect a variable resistance between Rint or Rext/Cext and Vcc. (This mode being used in circuit)

The other resisters and capacitors around the chip set the bias conditions needed to support this function. Values shown in the circuit are selected to allow device to operate in this standard mode. The 1uF capacitor sets the formula that can be used do the calculation. I have included parts of the data sheet at end of this documents for reference. The equation we want is:
Note: Be careful of units as equation expects input to have set exponents.

> Tw = 0.33 x Rt Cext
> Cext is 1uF or 1000000pF
> Rt = 4.7 + Pot + 4.7 So range is Low = 9.4 Center = 59.4 High =109.4
>
> Tw low = 3,102,000ns or 3.102msec
> Tw center =19,802,000ns or 19.802msec
> Tw high = 36,102,000ns or 36.102msec

When $C_{ext} \geq 1\ \mu F$, the output pulse width is defined as:

$$t_w = 0.33 \cdot R_T \cdot C_{ext}$$

For the above two equations, as applicable;

K is multiplier factor, see Figure 7
R_T is in kΩ (internal or external timing resistance)
C_{ext} is in pF
t_w is in ns

Cell off switch on front panel when in off position sets the state of the final AND IC in SN7408N to LOW. When the output signal is LOW there are no pulses generated.

The (K) Input is assumed to act like another switch input to turn cell off based on external events. As I have not reviewed function of that module, I have not verified that this is in fact the case. Other of drawings of this circuit do not show the (K) input so it appears it was added to support additional functions. I believe it may be used to turn cell off when pressure gets too high (this is just a guess).

Q11 2N3904 amplifies the output signal and feeds it to the following:

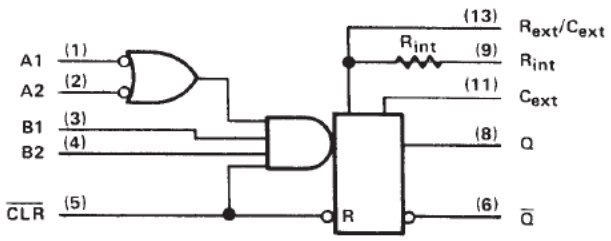
1. The Test Point on front panel
2. Lights the Green LED which also gets 10 VDC from an external source
3. Signal (A) to the VIC

Note: There are chips on the card that do not appear to be used by this circuit. Do not know why, it is possible that they supported a function no longer needed and card has not been updated. Just like the (K) input looks like it was added later.

Details of SN72122N from data sheet

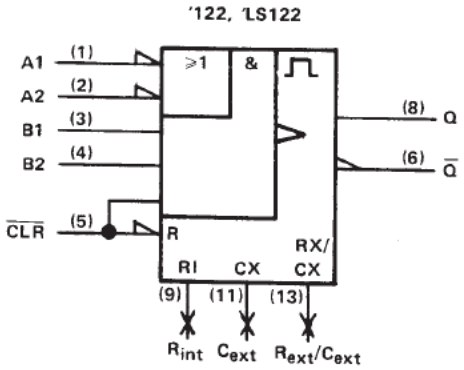
logic diagram (positive logic)

'122, 'LS122



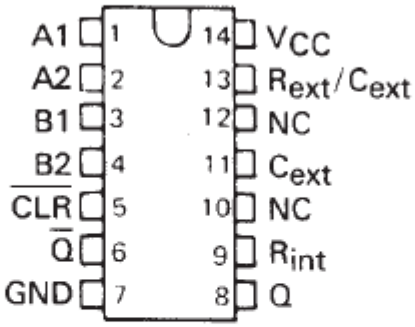
logic symbol†

'122, 'LS122



R_{int} is nominally 10 kΩ for '122 and 'LS122

SN54122, SN54LS122 . . . J OR W PACKAGE
SN74122 . . . N PACKAGE
SN74LS122 . . . D OR N PACKAGE
(TOP VIEW) (SEE NOTES 1 THRU 4)



NOTES:
1. An external timing capacitor may be connected between C_{ext} and Re_{xt}/C_{ext} (positive).
2. To use the internal timing resistor of '122 or 'LS122, connect R_{int} to V_{CC}.
3. For improved pulse duration accuracy and repeatability, connect an external resistor between R_{ext}/Ce_{xt} and V_{CC} with R_{int} open-circuited.
4. To obtain variable pulse durations, connect an external variable resistance between R_{int} or R_{ext}/C_{ext} and V_{CC}.

description

These d-c triggered multivibrators feature output pulse-duration control by three methods. The basic pulse time is programmed by selection of external resistance and capacitance values (see typical application data). The '122 and 'LS122 have internal timing resistors that allow the circuits to be used with only an external capacitor, if so desired. Once triggered, the basic pulse duration may be extended by retriggering the gated low-level-active (A) or high-level-active (B) inputs, or be reduced by use of the overriding clear. Figure 1 illustrates pulse control by retriggering and early clear.

The 'LS122 and 'LS123 are provided enough Schmitt hysteresis to ensure jitter-free triggering from the B input with transition rates as slow as 0.1 millivolt per nanosecond.

The R_{int} in nominall 10 kΩ for '122 and 'LS122.

When $C_{ext} \geq 1\ \mu F$, the output pulse width is defined as:

$$t_w = 0.33 \cdot R_T \cdot C_{ext}$$

For the above two equations, as applicable;

K is multiplier factor, see Figure 7
R_T is in kΩ (internal or external timing resistance)
C_{ext} is in pF
t_w is in ns

For maximum noise immunity, system ground should be applied to the C_{ext} node, even though the C_{ext} node is already tied to the ground lead internally. Due to the timing scheme used by the 'LS122 and 'LS123, a switching diode is not required to prevent reverse biasing when using electolytic capacitors.

MULTIPLIER FACTOR
vs
EXTERNAL CAPACITOR

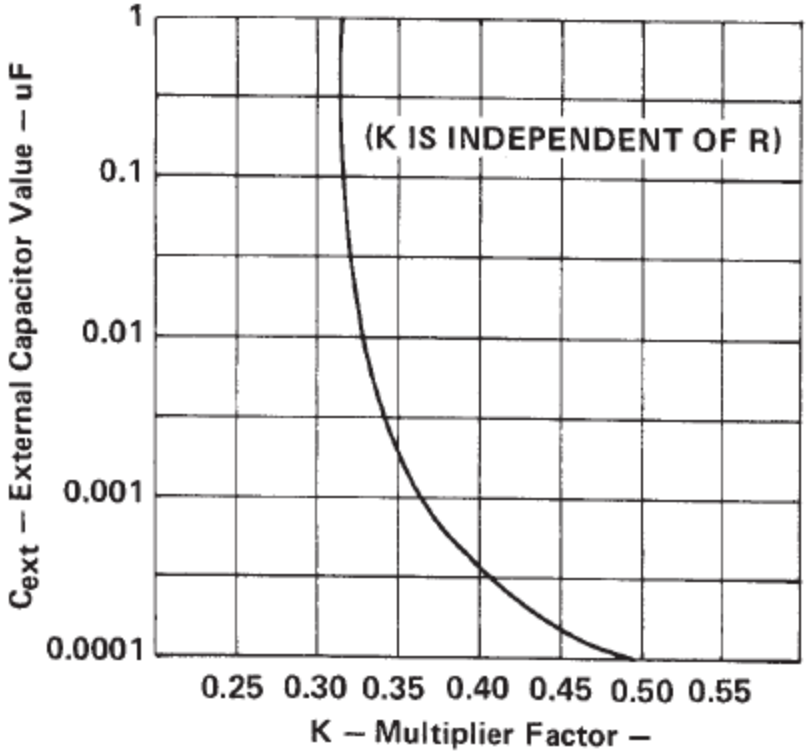


FIGURE 7

The basic output pulse duration is essentially determined by the values of external capacitance and timing resistance. For pulse durations when $C_{ext} \leq 1000$ pF, use Figure 6, or use Figure 7 where the pulse duration may be defined as:

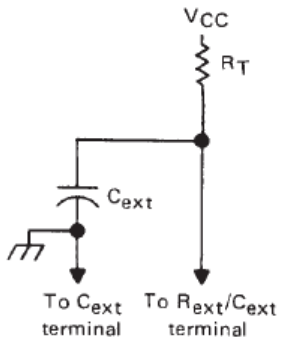
$$t_w = K \cdot R_T \cdot C_{ext}$$

When $C_{ext} \geq 1\ \mu F$, the output pulse width is defined as:

$$t_w = 0.33 \cdot R_T \cdot C_{ext}$$

For the above two equations, as applicable;

K is multiplier factor, see Figure 7
R_T is in kΩ (internal or external timing resistance)
C_{ext} is in pF
t_w is in ns



TIMING COMPONENT CONNECTIONS

FIGURE 5